1. A decoding circuit comprising:

an input unit for entering coded digital signals in parallel in accordance with a number of interleaved codes;

a processor, said processor in turn comprising an error locator polynomial calculator and an error value polynomial calculator, for processing data obtained serially from said interleaved codes that are received by said input unit; and

an output unit for correcting errors by employing output data that is received serially from said processor and said digital signals, and for outputting the obtained digital signals in parallel in accordance with said number of interleaved codes.

2. The decoding circuit according to claim 1, wherein said input unit calculates syndromes for said input digital signals, and transmits said syndromes for interleaved codes to said processor serially;

wherein said processor employs said syndromes to calculate coefficients of an error locator polynomial and coefficients of an error value polynomial; and

wherein said output unit, based on said coefficients of said error locator polynomial and said coefficients of said error value polynomial received from said processor, generates error locations and error values, using a linear calculation in a Galois extension field for said input digital signals, and defines said error locations and said error values as said digital signals to be output.

3. The decoding circuit according to claim 1, wherein said input digital signals are Reed-Solomon codes that are received in parallel through an i-channel, and the decoding circuit comprises at least one of a multiplexer and a demultiplexer, having a ratio of one of i:1 and 1:i.

4. The decoding circuit according to claim 1, wherein, for optical communication, wavelength division multiplexing is used for the transmission of said input digital signals.

5. The decoding circuit according to claim 1, wherein said input unit comprises a sequential circuit and said processor comprises a combinational circuit.

6. The decoding circuit according to claim 1 that is used for at least one of the correction of digital signal errors and encryption.

7. A decoder comprising:

input means, for receiving coded digital signals;

processing means, for processing said coded digital signals and for calculating coefficients of an error locator polynomial and coefficients of an error value polynomial; and

output means, for outputting digital signals for which errors have been corrected using said coefficients of said error locator polynomial and said coefficients of error value polynomial,

wherein said input means receives in parallel, in

accordance with a number of interleaved codes, said coded digital signals, and employs said coded digital signals to calculate syndromes as data obtained serially from said interleaved codes,

wherein said processing means employs said syndromes output by said processing means to calculate said coefficients of said error locator polynomial and said coefficients of said error value polynomial, and

wherein said output means employs said coefficients of said error locator polynomial, said coefficients of said error value polynomial and said coded input digital signals to correct errors using a linear calculation in a Galois extension field, and outputs in parallel the obtained digital signals in accordance with said number of interleaved codes.

8. The decoder according to claim 7, wherein said input digital signals are Reed-Solomon codes that are received in parallel through an i-channel, and the decoder comprises at least one of a multiplexer and a demultiplexer having a ratio of one of i:1 or 1:i.

9. The decoder according to claim 7, wherein, for optical communication, wavelength division multiplexing is used for transmission of said input digital signals.

10. The decoder according to claim 7, wherein said input unit comprises a sequential circuit and said processor comprises a combinational circuit.

11. The decoder according to claim 7 that is used for at least one of the correction of digital signal errors and encryption.

12. A method for decoding a digital signal comprising:

an input step of entering coded digital signals in parallel in accordance with a number of interleaved codes;

a process step of employing a processor, including an error locator polynomial calculator and an error value polynomial calculator, to process data obtained serially from said interleaved codes that are received at said input unit;

a generation step of employing said output data that is received from said processor and said digital signals to generate digital signals for which an error has been corrected; and

an output step of outputting the obtained digital signals in parallel in accordance with said number of interleaved codes.

13. The decoding method according to claim 12, wherein said input step includes the step of:

calculating syndromes for said input digital signals, and transmitting said syndromes to said processor as data obtained serially from interleaved codes,

wherein said process step includes the step of:

employing said syndromes to calculate coefficients of an error locator polynomial and coefficients of an error

value polynomial, and

wherein said output step includes the step of:

based on said coefficients of said error locator polynomial and said coefficients of said error value polynomial received from said processor, generating error locations and error values, using a linear calculation in a Galois extension field for said input digital signals, and defining said error locations and said error values as said digital signals to be output.

14. The decoding method according to claim 12, further comprising:

a i:1 multiplexing step and a 1:i demultiplexing step, wherein said input step includes the step of:

receiving said input digital signals that are Reed-Solomon codes in parallel through an i-channel.

15. The decoding method according to claim 12, wherein, for optical communication, wavelength division multiplexing is used for the transmission of said input digital signals.

16. The decoding method according to claim 12, wherein said input step is used for the calculation using a sequential circuit and said process step is used for the calculation using a combinational circuit.

17. The decoding method according to claim 12 that is used for at least one of the correction of digital signal errors and encryption.

18. A semiconductor device used to process a digital signal, said device comprising:

input means, for receiving coded digital signals;

processing means, for processing said coded digital signals and for calculating coefficients of an error locator polynomial and coefficients of an error value polynomial; and

output means, for outputting digital signals for which errors have been corrected using said coefficients of said error locator polynomial and said coefficients of said error value polynomial,

wherein said input means receives in parallel, in accordance with the number of interleaved codes, said coded digital signals, and employs said coded digital signals to calculate syndromes as data obtained serially from interleaved codes,

wherein said processing means employs said syndromes output by said input means to calculate said coefficients of said error locator polynomial and said coefficients of said error value polynomial, and

wherein said output means employs said error location, said error value and said coded input digital signals to perform an operation in a Galois extension field, and outputs in parallel the obtained digital signals in accordance with said number of interleaved codes.

19. The semiconductor device according to claim 18, further comprising:

at least one of a multiplexer and a demultiplexer, having a ratio one of i:1 and 1:i, wherein said input digital signals are Reed-Solomon codes that are received in parallel through an i-channel.

20. The semiconductor device according to claim 18, wherein, for optical communication, wavelength division multiplexing is used for the transmission of said input digital signals.

21. The semiconductor device according to claim 18, wherein said input means comprises a sequential circuit and said processing means comprises a combinational circuit.